

In a multiprocessor system including numbers of processors which realizes hierarchical interprocessor communication and enables high-speed interprocessor communication, each processing element is composed of a plurality of processors physically sharing the same register file, and in the processing element, interprocessor communication is conducted by sharing the register. Every several processing elements are connected to the same local bus and the local buses are connected to each other by a bridge and a global bus. Between processing elements located at a short distance from each other, communication is conducted through one local bus, while between processing elements located at a long distance from each other, communication is conducted through a plurality of local buses and global buses.

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